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1. A method for forming a metal silicide layer in a semiconductor device comprising:

forming a first gate structure including a first gate electrode and a first spacer on a first region of a substrate;

forming a second gate structure including a second gate electrode and a second spacer on a second region of the substrate;

partially removing the first and second spacers to different depths such that side portions of the first and second gate electrodes are exposed by different amounts in thickness; and

forming a metal silicide layer on the first and second electrodes having the different exposed thicknesses,

wherein the metal silicide layer formed on the second gate electrode has a second thickness that is different from a first thickness of the metal silicide layer formed on the first gate electrode.

2. The method of claim 1, wherein the first gate structure corresponds to a gate structure of an N type MOS transistor, and the second gate structure corresponds to a gate structure of a P type MOS transistor.

3. The method of claim 1, wherein a first impurity region is formed in the first region of the substrate adjacent to the first gate structure, prior to partially removing

4. The method of claim 1, wherein partially removing the first and second spacers comprises:

partially removing the second spacer to expose upper side portions of the second electrode; and

simultaneously and partially removing the first and second spacers to provide the first and second gate electrodes having the different exposed thicknesses;

wherein the second thickness of the metal silicide layer formed on the second gate electrode is greater than the first thickness of the metal silicide layer formed on the first gate electrode.

5. The method of claim 4, wherein the exposed thickness of the first gate electrode is about 100Å to about 300Å, and the exposed thickness of the second gate electrode is about 100Å to about 1,000 Å.

7. The method of claim 6, wherein the exposed thickness of the first gate electrode is about 100Å to about 300Å, and the exposed thickness of the second gate electrode is about 100Å to about 1,000 Å.

8. A method for forming a metal silicide layer in a semiconductor device comprising:

forming a first gate structure including a first gate electrode and a first spacer on a first region of a substrate;

forming a second gate structure including a second gate electrode and a second spacer on a second region of the substrate;

partially removing the second spacer to partially expose upper side portions of the second gate electrode;

removing partially and simultaneously the first and second spacers; and

forming a metal silicide layer on the first and second gate electrodes,

wherein a second thickness of the metal silicide layer formed on the second gate electrode is greater than a first thickness of the metal silicide layer formed on the first gate electrode.

9. The method of claim 8, wherein a first impurity region is formed in the first

region of the substrate adjacent to the first gate structure prior to partially removing the second spacer, and wherein a second impurity region is formed in the second region of the substrate adjacent to the second gate structure prior to removing partially and simultaneously the first and second spacers.

10. The method for forming a metal silicide layer in a semiconductor device of claim 9, wherein forming the first impurity region comprises:

forming a first photoresist pattern on the substrate to expose the first region of the substrate; and

doping a first impurity into the first region of the substrate using the first photoresist pattern as a first mask; and

wherein forming the second impurity region comprises:

forming a second photoresist pattern on the substrate to expose the second region of the substrate; and

doping a second impurity into the second region of the substrate using the second photoresist pattern as a second mask.

11. The method of claim 10, wherein the first gate structure corresponds to a gate structure of an N type MOS transistor, and the second gate structure corresponds to a gate structure of a P type MOS transistor.

12. The method of claim 8, wherein the second spacer is removed by a thickness of about 100Å to about 500Å, and the first and second spacers are simultaneously removed by a thickness of about 100Å to about 300Å.